

In re Patent Application of:  
**CAVALLI**  
Serial No. 09/826,427  
Filing Date: April 3, 2001

REMARKS

The Examiner is thanked for the thorough examination of the present application. Independent Claims 1, 7, 11, and 17 have been amended to more clearly define the subject matter thereof over the prior art. Support for the amendments may be found on page 5, lines 24-29 of the originally filed specification, for example. No new matter is being added. Dependent Claims 18 and 20 have been amended for consistency with the changes to Claim 17. Also, dependent Claims 15 and 16 have been amended to correct the minor informalities, as helpfully pointed out by the Examiner.

In view of the amendments and the supporting arguments presented in detail below, it is submitted that all of the claims are patentable.

I. The Claimed Invention

The present invention is directed to a method for processing an interrupt request using a microprocessor executing a program. As recited in amended independent Claim 7, for example, the method includes detecting the interrupt request and storing contextual data of the program. Moreover, after the contextual data is stored, it is then verified that the interrupt request is still present. If it is not, then execution of the program is resumed. On the other hand, if the presence of the interrupt request is verified, then an interrupt acknowledge signal is sent, and the microprocessor switches to an interrupt subroutine. As such, the microprocessor advantageously avoids unnecessary resets or malfunctions caused by a false or withdrawn interrupts.

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Independent Claim 1 is directed to a similar method, and independent Claims 11 and 17 are directed to related microprocessors. Similar to Claim 7, each of these claims also recites the verification of whether the interrupt request is still present after storing the program contextual data prior to taking further action.

## II. The Claims Are Patentable

The Examiner rejected independent Claims 7 and 17 over U.S. Patent No. 4,484,271 to Miu et al., and Claims 1 and 11 stand rejected based upon Miu et al. in view of a textbook by Short. Miu et al. discloses a microprocessor system with a hardware interrupt apparatus. The Examiner contends that Miu et al. teaches that, after detecting an interrupt request and storing contextual data of the program being run when the interrupt was received, verification that the interrupt is still present is performed. As support, the Examiner points to col. 78, lines 22-26 of Miu et al., and he states that "after the first interrupt request is processed, a check is performed (verification) to see if the interrupt request signal is still provided so that further interrupts can be processed without returning to the originally interrupted program." Office Action, pages 3-4. The Examiner cites the Short textbook because it teaches storing context information in a stack.

The above-noted independent claims have been amended to more clearly recite that the verification is to determine if the originally detected interrupt is still present after the microprocessor stores the contextual data of the program so that

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it can later return to processing that program. That is, the verification is for determining if the same interrupt is still present when the microprocessor is ready and able to act upon it. As discussed in the background of the originally filed specification, a typical prior art microprocessor might malfunction if it attempted to process an interrupt which was no longer present (e.g., because it was withdrawn or it was a false, ephemeral "interrupt" caused by an electromagnetic disturbance), or instead act upon a default reset interrupt request to avoid such a malfunction. However, as recited in the above-noted claims, verification that the interrupt is still present is advantageously performed so that the interrupt request can be processed accordingly if it is present, or the original program can be resumed if it is not, to thus reduce occurrences of malfunctions or unwanted resets.

The paragraph from Miu et al. relied upon by the Examiner is as follows:

"A further examination of FIG. 42 will reveal that at the end of the second hardware interrupt service microroutine, if there are no further hardware interrupts pending, control will be returned to the microinstruction whose address is stored in hardware interrupt return register 252 thus returning control to the original microprogram at the point that it was interrupted by the first hardware interrupt. Thus it can be seen that back-to-back (i.e., consecutive) hardware interrupts can be serviced without returning to the interrupted original microprogram between the first and second hardware interrupt service microroutines." Miu et al., col. 78, lines 15-26.

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This text simply teaches that as one interrupt is completed, the CPU checks to see if another, different interrupt(s) is pending and, if not, it returns to the program it was performing before the first interrupt was received. Nowhere does Miu et al. teach or fairly suggest that, after detecting the presence of an interrupt signal and storing program contextual data, verification is performed to determine if the same interrupt signal is still present before taking further action. Neither do the teachings of Short nor any of the remaining prior art of reference taken in combination with those of Miu et al. as a whole teach or fairly suggest the noted deficiency. As such, it is respectfully submitted that the rejection of the above-noted independent claims should be withdrawn.

Accordingly, it is submitted that independent Claims 1, 7, 11, and 17 are patentable over the prior art. Their respective dependent claims, which recite yet further distinguishing features, are also patentable over the prior art and require no further discussion herein.

#### CONCLUSIONS

In view of the foregoing, it is submitted that all of the claims are patentable. Accordingly, a Notice of Allowance is respectfully requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

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Respectfully submitted,



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